APPLICATION NOTE

AN1891

SA8025 Fractional-N synthesizer for 2GHz band applications

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INTRODUCTION

The SA8025 is a 3V, 1.8GHz, SSOP 20-pin packaged fractional-N phase locked-loop (PLL) frequency synthesizer. It is targeted for systems like the Japan Personal Handy Phone System (PHS, formerly PHP) which demands fast switching time and good noise performance. Built on the QUBiC BiCMOS process, it has phase detectors with maximum frequency of 5MHz and an auxiliary synthesizer that can operate up to 150MHz. This design was based on the UMA1005 (all CMOS), an earlier version fractional-N synthesizer which requires an external prescaler for 1 and 2GHz applications. There is also a 1GHz version fractional-N PLL frequency synthesizer, the SA7025, available for systems operating under 1GHz. One should expect the performance of the SA8025 and SA7025 to be comparable to the UMA1005 with an extra prescaler. This application note will serve as a supplement to the application note for the UMA1005 (Report No: SCO/AN92002) or as a stand-alone document specifically for the SA8025.

OVERVIEW OF THE FRACTIONAL-N FREQUENCY SYNTHESIZER

Figure 1 shows the basic building blocks of a PLL frequency synthesizer. It consists of a programmable reference divider, phase detector and programmable RF divider (prescaler and main divider). The low-pass filter and voltage-controlled oscillator (VCO) are external to provide design flexibility. The loop has a self-correction mechanism which forces comparison frequency $f_{COMP} = f_{COMP'}$. Since $f_{COMP} = f_{REF}/M$ and $f_{COMP}' = f_{VCO}/N$, the desired frequency becomes $f_{VCO} = (f_{REF}/M)N$. M (reference divider) is fixed for generating f_{COMP}. By incrementing or decrementing the value of N, different frequencies can be synthesized.

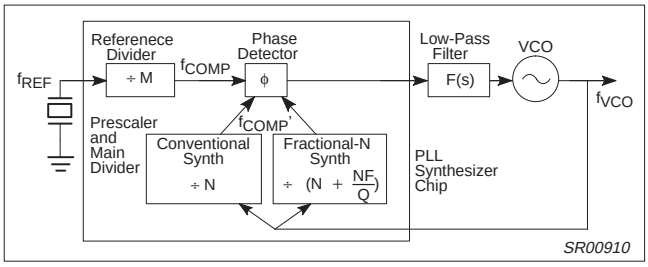

Figure 1. PLL Synthesizer

For conventional synthesizers, the phase detector comparison frequency must be equal to the channel spacing (frequency resolution) because the main divider (N) can only increment and decrement in integer steps. However, the main divider of the fractional-N synthesizer is capable of generating steps to be a fraction of the comparison frequency. Now the total divider ratio consists of an integer part (N) and a fractional part (NF/Q). The numerator (NF) and the denominator (Q, either 5 or 8) of a fraction are controlled through software programming.

Referring to Figure 2, to synthesize channels 1680MHz, 1680.3MHz and 1680.6MHz with channel spacing of 300kHz, the values have to be 5600MHz, 5601MHz and 5602MHz, respectively. The channel spacing of a fractional-N synthesizer is a fraction of the comparison frequency. When using the SA8025, the comparison frequency is increased to either 1.5MHz (mod 5) or 2.4MHz (mod 8), yielding a smaller N value of 1120 (mod 5) or 700 (mod 8) to synthesize 1680MHz.

The advantage of fractional-N synthesizers is two-fold. Since the close-in noise floor is directly related to total divide ratio (N), reducing N five or eight times theoretically implies a close-in noise floor improvement of 14dB (20log(5)) or 18dB (20log(8)), respectively. At the same time, the comparison breakthrough will be 5 or 8 times further away than it would be if a conventional synthesizer were used. This allows a wider loop filter to be used, thus achieving a faster switching time. Faster switching is also achieved due to the higher number of comparison cycles.

To synthesize 1680, 1680.3, 1680.6MHz with channel spacing = 300kHz

Conventional syn. $f_{VCO} = f_{COMP}$ (N)	SA8025 (mod 5) $f_{VCO} = f_{COMP}$ (N + NF/5)	SA8025 (mod 8) $f_{VCO} = f_{COMP}$ (N + NF/8)
1680 = 0.3 (5600)	1680 = 1.5 (1120 + 0/5)	1680 = 2.4 (700 + 0/8)
1680.3 = 0.3 (5601)	1680.3 = 1.5 (1120 + 1/5)	1680.3 = 2.4 (700 + 1/8)
1680.6 = 0.3 (5602)	1680.6 = 1.5 (1120 + 2/5)	1680.6 = 2.4 (700 + 2/8)
$f_{COMP} = f_{CH} = 0.3MHz$	$f_{COMP} = 5 \times f_{CH} = 1.5MHz$	$f_{COMP} = 8 \times f_{CH} = 2.4MHz$

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Figure 2. What Is Fractional-N?

DESIGNING WITH THE SA8025

Reference Signal and Divider

Since the synthesized signal is derived from the reference signal, using a clean crystal with an appropriate level is crucial. The reference signal should be AC coupled and deliver between 300 and $600mV_{P-P}$ to Pin 8 for the input buffer to convert it into a CMOS compatible level. The maximum crystal frequency the part can handle is determined by both analog and digital supplies because the input buffer and the reference divider are powered by V_{DDA} and V_{DD}, respectively. For a $V_{DD} = V_{DDA} = 3V$ configuration, the maximum crystal frequency allowed is 20MHz. When $V_{DD} = 3V$ and $V_{DDA} = 5V$, this frequency becomes 30MHz.

Phase Detector and Charge Pumps

The main and auxiliary phase detectors (see Figure 3) detect both the phase and frequency difference between the divided-down VCO and reference signals. If the main/aux leads the reference, there will be a pulse coming out of the phase detector which turns on the N-type charge pump and sinks current from the low-pass filter. On the other hand, if the main/aux lags the reference, the P-type charge pump will be activated and more current will be delivered to the low-pass filter.

Due to the internal delays of CMOS devices, the phase comparator needs a minimum phase difference, backlash time, to generate an output pulse. This backlash time will introduce a dead-zone around zero phase difference where a small phase error cannot be detected. The way the SA8025 eliminates this problem is by having a minimum on-time of $1/f_{REF}$ for the P pump (sourcing) and N pump (sinking) when the loop is in lock condition, which is shown in Figure 4. Since the charge pump on-time is determined by the crystal reference frequency (f_{REF}), the higher the frequency, the better will be the close-in noise performance. Typically, there will be 3dB close-in noise improvement for a 50% increase in reference frequency (e.g., from 9.6 to 14.4MHz).

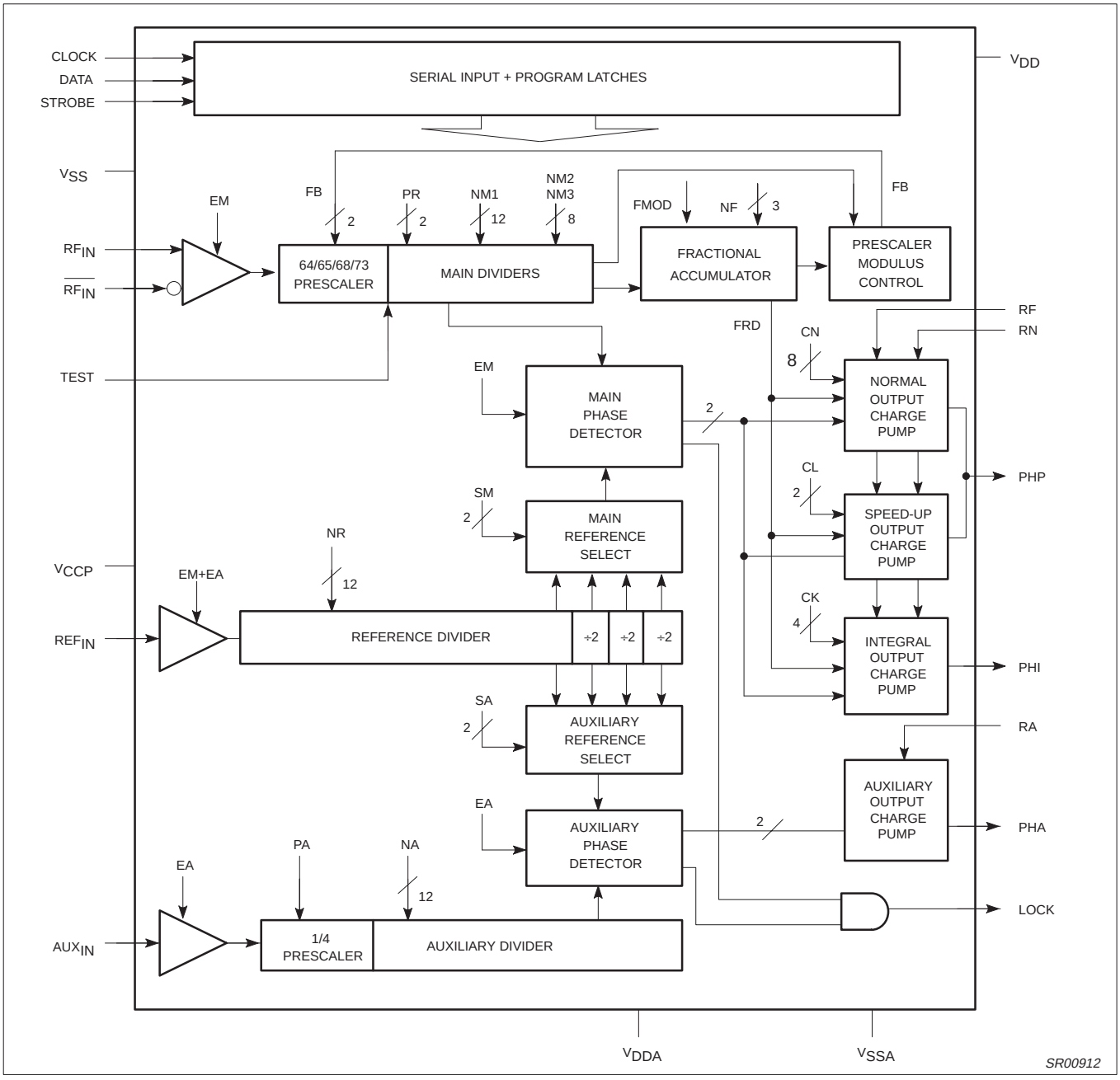

Figure 3. Block Diagram of the SA8025

Since the phase detector detects phase from –2π to 2π, its gain (K_ϕ) equals the charge pump output current (I_{CP}) divided by 2π with units of A/rad.

The charge pump output current, I_{CP} (A), is determined by the external resistor RN and the internal registers CN, CK and CL values. The I_{CP} for normal mode operation (PHP pump only) is:

$$I_{CP} = \frac{CN \cdot I_{RN}}{32} \quad \text{(EQ. 1)}$$

where $$RN = \frac{V_{DDA} - 0.9 - 150(I_{RN})^{0.5}}{I_{RN}} \quad \text{(EQ. 2)}$$

Figure 5 shows a graphical representation of Eq. 2. The curves are valid for both main and aux synthesizers. Notice that in normal mode, currents due to the CK and CL values are negligible and only the PHP pump is activated. When the part is in speed-up, both charge pumps are on and the I_{CP} for PHP is:

$$I_{CP} = \frac{CN \cdot I_{RN}}{32} (2^{CL+1} + 1) \quad \text{(EQ. 3)}$$

I_{CP} for PHI is:

$$I_{CP} = \frac{CN \cdot I_{RN}}{32} (2^{CL+1}) \, CK \quad \text{(EQ. 4)}$$

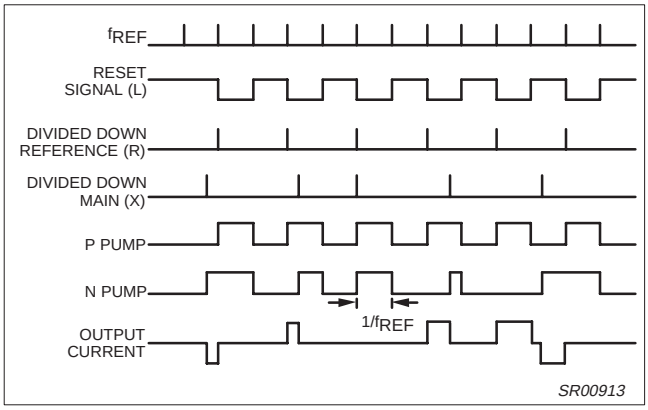

Figure 4. Phase Detector Timing Diagram

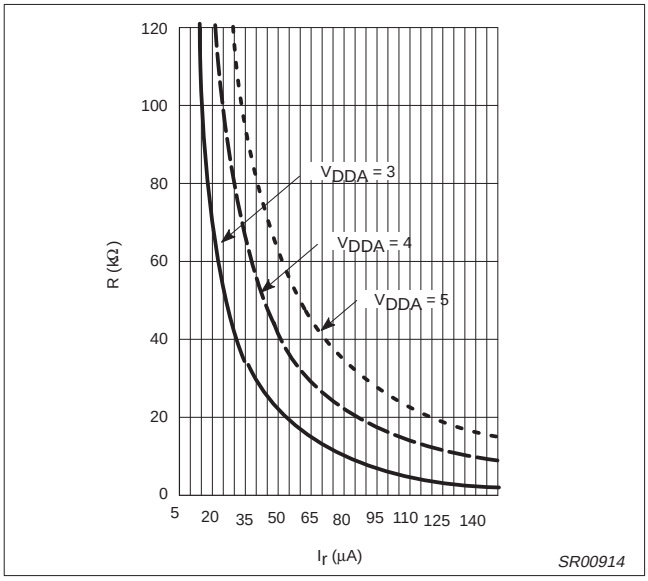

Figure 5. RN(RA) vs. $I_{RN}(I_{RA})$ for Different V_{DDA}

From Eq. 3 notice that in speed-up mode, the PHP output current will be at least 3 times higher than the normal mode current even though CL=0. Speed-up mode stays active as long as the STROBE signal is high after an A word is sent.

Bypass capacitors (100nF) should be used for RN, RF and RA pins to prevent high frequency noise being coupled into the pins causing modulation of the VCO.

Main Divider

The total divide ratio, N, is determined by the combination of the main divider ratio (NM1, NM2, NM3, NM4) and the prescaler values. The part is internally controlled to produce division ratios of N or N+1 when a fractional function is used. The minimum divide ratio, N', which guarantees that all the channels above this ratio can be synthesized consecutively (no blind channels) is different for each prescaler ratio. Since the fractional-N synthesizer increases the comparison frequency, lower N values can be used. To accomplish this, the SA8025 uses a 4 modulus (64/65/68/73) prescaler that lowers the minimum divide ratio to 933.

When programming a total divide ratio (N) which has no components of NM3 or NM4, simply treat them as "don't cares".

Using divide ratios below the minimum divide ratio (N') to synthesize channels is possible, but it requires trial and error. For instance, in the Japan Personal Handy Phone System (PHS), the VCO is running at 1646.7 to 1670.1MHz (248.45MHz first IF). Using a modulus 8 fraction with 300kHz channel spacing, the required N value is between 686 and 695, which is less than the N' of the 4 modulus prescaler. Calculation showed that only N = 695 is not obtainable using the 4 modulus prescaler, but it can be obtained using the 64/65/73 prescaler. The B word must be sent to change the prescaler ratio.

Table 1.

Prescaler Ratio	PR Bits	N'	Total Divide Ratio, N
64/65	01	4032	$N = (NM1 + 2) \times 64 + NM2 \times 65$
64/65/68	10	1348	$N = (NM1 + 2) \times 64 + NM2 \times 65 + (NM3 + 1) \times 68$
64/65/68/73	11	933	$N = (NM1 + 2) \times 64 + NM2 \times 65 + (NM3 + 1) \times 68 + (NM4 + 1) \times 73$
64/65/73	00	1096	$N = (NM1 + 2) \times 64 + NM2 \times 65 + (NM4 + 1) \times 73$

Determining the Programming Values for NM1, NM2, NM3 and NM4

For the 2-modulus prescaler (64/65), NM1 and NM2 can be determined by:

$$NM2 = 64 \cdot FRAC\left(\frac{N}{64}\right) \quad \text{(EQ. 5)}$$

$$NM1 = INT\left(\frac{N}{64}\right) - NM2 - 2 \quad \text{(EQ. 6)}$$

where FRAC (...) and INT (...) takes the fractional integer part of the argument.

For the 3-modulus prescaler, NM1, NM2 and NM3 (NM4 when PR = 00) can be determined by:

$$K1 = INT\left(\frac{N - R}{64}\right) - 3, \quad K2 = FRAC\left(\frac{N-R}{64}\right) \cdot 64 \quad \text{(EQ. 7)}$$

$$NM3 = INT\left(\frac{K2}{R}\right) \quad \text{(EQ. 8)}$$

$$NM2 = FRAC\left(\frac{K2}{R}\right) \cdot R \quad \text{(EQ. 9)}$$

$$NM1 = K1 - NM2 - NM3 \quad \text{(EQ. 10)}$$

where R = 4 for 64/65/68 prescaler, R = 9 for 64/65/73 prescaler.

For the 4-modulus prescaler (64/65/68/73), we first arbitrarily choose NM4 (smaller values are preferable) and then use the following formulas to calculate NM1, NM2 and NM3:

$$K1 = INT\left(\frac{N - 13}{64}\right) - 4, \; K2 = FRAC\left(\frac{N-13}{64}\right) \cdot 64 \quad \text{(EQ. 11)}$$

$$NM3 = INT\left(\frac{K2 - 9 \cdot NM4}{4}\right) \quad \text{(EQ. 12)}$$

$$NM2 = FRAC\left(\frac{K2 - 9 \cdot NM4}{4}\right) \cdot 4 \quad \text{(EQ. 13)}$$

$$NM1 = K1 - NM2 - NM3 - NM4 \quad \text{(EQ. 14)}$$

Notice that the formulas shown above will give only one set of NM1, NM2, NM3 and NM4 that generates the desired N value. Generating continuous N below 933 (4 modulus) is still possible if all

four modulus options are used. It was found that the part can generate N continuously from 702. The program “8025NMIN.EXE”, provided with the “UMAWINE.EXE” for controlling the SA8025 demoboard, calculates all the N values that the part can generate. Users should run the program to find out the right NM1, NM2, NM3 and NM4 if N value of less than 702 is needed. This program will give only one possible combination of NM1 to NM4 for each N.

```
program sa8025
Philips Semiconductors, Sunnyvale, CA
Author: Wing S. Djen
Date: 5/9/94
Purpose: To find the minimum divide ratio on the SA8025

integer i, n1, n2, n3, n4, mod2, mod3a, mod3b, mod4,
+              delta1, delta2, delta3, delta4,
+              temp2, temp3a, temp3b, temp4
+              lown, highn

write(*,*) 'Enter the lowest N value→'
read(*,*) lown
write(*,*) 'Enter the highest N value→'
read(*,*) highn
do 10 i=lown, highn
do 10 n1=0,10
do 10 n2=0,10
do 10 n3=0,10
do 10 n4=0,10
    mod2 = (n1+2)*64 + n2*65
    mod3a = (n1+2)*64 + n2*65 + (n3+1)*68
    mod3b = (n1+2)*64 + n2*65 + (n4+1)*73
    mod4 = (n1+2)*64 + n2*65 + (n3 + 1)*68 + (n4+1)*73
   delta1 = i-mod2
   delta2 = i-mod3a
   delta3 = i-mod3b
   delta4 = i-mod4
   if (delta1.eq.0) then
     if (temp2.eq.mod2) goto 1
     write(*,5) mod2, n1, n2
5    format(' PR="01"  N=',i5,3x,'NM1',i2,3x,
+             'NM2=',i2)
     temp2=mod2
     endif
1    if (delta2.eq.0) then
     if (temp3a.eq.mod3a) goto 2
     write(*,6) mod3a, n1, n2, n3
6    format(' PR="10"  N=',i5,3x,'NM1',i2,3x,
+             'NM2=',i2,3x,'NM3=',i2)
     temp3a=mod3a
     endif
2    if (delta3.eq.0) then
     if (temp3b.eq.mod3b) goto 3
     write(*,7) mod3b, n1, n2, n4
7    format(' PR="00"  N=',i5,3x,'NM1',i2,3x,
+             'NM2=',i2,3x,'NM4=',i2)
     temp3b=mod3b
     endif
3    if (delta4.eq.0) then
     if (temp4.eq.mod4) goto 10
     write(*,8) mod4, n1, n2, n3, n4
8    format(' PR="11"  N=',i5,3x,'NM1',i2,3x,
+             'NM2=',i2,3x,'NM3=',i2,3x,'NM4=',i2)
     temp4=mod4
     endif
10   continue
     end
```

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The following is a sample output of the “8025NMIN.EXE” program. It shows the divide ratios that cover the PHS band.

PR="01"	N=128	NM1=0	NM2=0		
PR="01"	N=192	NM1=1	NM2=0		
PR="01"	N=193	NM1=0	NM2=1		
:	:	:	:		
:	:	:	:		
PR="11"	N=679	NM1=0	NM2=1	NM3=4	NM4=1
PR="00"	N=679	NM1=1	NM2=3	NM4=3	
PR="00"	N=680	NM1=0	NM2=4	NM4=3	
PR="11"	N=680	NM1=1	NM2=1	NM3=2	NM4=2
PR="11"	N=681	NM1=0	NM2=2	NM3=2	NM4=2
PR="11"	N=682	NM1=0	NM2=0	NM3=5	NM4=1
PR="11"	N=683	NM1=0	NM2=3	NM3=0	NM4=3
PR="11"	N=684	NM1=0	NM2=1	NM3=3	NM4=2
PR="11"	N=685	NM1=1	NM2=1	NM3=1	NM4=3
PR="00"	N=685	NM1=3	NM2=0	NM4=4	
PR="11"	N=686	NM1=0	NM2=2	NM3=1	NM4=3
PR="00"	N=686	NM1=2	NM2=1	NM4=4	
PR="11"	N=687	NM1=0	NM2=0	NM3=4	NM4=2
PR="00"	N=687	NM1=1	NM2=2	NM4=4	
PR="00"	N=688	NM1=0	NM2=3	NM4=4	
PR="11"	N=688	NM1=1	NM2=0	NM3=2	NM4=3
PR="11"	N=689	NM1=0	NM2=1	NM3=2	NM4=3
PR="11"	N=690	NM1=1	NM2=1	NM3=0	NM4=4
PR="11"	N=691	NM1=0	NM2=2	NM3=0	NM4=4
PR="11"	N=692	NM1=0	NM2=0	NM3=3	NM4=3
PR="11"	N=693	NM1=1	NM2=0	NM3=1	NM4=4
PR="11"	N=694	NM1=0	NM2=1	NM3=1	NM4=4
PR="00"	N=694	NM1=2	NM2=0	NM4=5	
PR="00"	N=695	NM1=1	NM2=1	NM4=5	
PR="00"	N=696	NM1=0	NM2=2	NM4=5	
PR="11"	N=697	NM1=0	NM2=0	NM3=2	NM4=4
PR="11"	N=698	NM1=1	NM2=0	NM3=0	NM4=5
PR="11"	N=699	NM1=0	NM2=1	NM3=0	NM4=5
PR="11"	N=702	NM1=0	NM2=0	NM3=1	NM4=5

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RF Inputs

The RF inputs were designed to be used differentially for better noise rejection. However, the part can also be driven single-endedly with RF_{IN}+ or RF_{IN}– pin terminated by a 1nF capacitor. The matching network between VCO and RF input was intended for matching both the VCO and the Main Out on the demoboard to 50Ω (see Figure 6).

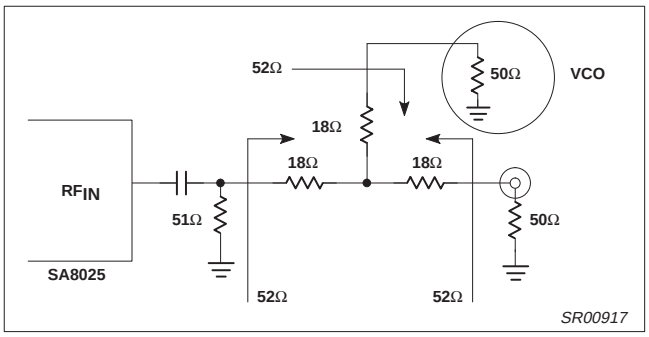

Figure 6. Matching Network for the RF_{IN} Pin

Lock Detect

The LOCK pin is selectable by software to be either the lock detect indicator, output of the main divider, output of the reference divider, or output of the auxiliary divider. Programming details can be found in the data sheet. The pin voltage will go to V_{DD} once the lock condition has been satisfied. Upon power up, the part is in an unknown state and the LOCK pin may go high. It will be functional only after the part is programmed.

Auxiliary Synthesizer

The auxiliary synthesizer does not have fractional-N capability. Therefore, its close-in phase noise and comparison breakthrough performance is comparable to that of a conventional synthesizer. However, this type of performance is not necessary for creating an offset frequency for a Frequency Division Duplex (FDD) system or the 2nd LO in a dual-conversion receiver. Also, an FM signal (e.g., GFSK or analog FM) can be obtained by directly frequency modulating the auxiliary VCO in a PLL structure. The auxiliary phase detector has the same bandwidth (5MHz) as the main phase detector. Current setting for the charge pump (I_{RA}) can be calculated using Eq. 2 and Figure 5. The charge pump output current (I_{CP}) becomes

$$I_{CP} = 8 \cdot I_{RA} \quad \text{(EQ. 15)}$$

Fractional Spurs and Compensation

The total divide ratio of the SA8025 is constantly changing between N and N + 1 to achieve fractional-N capability. This effect introduces an instantaneous phase error at the output of the phase detector in lock condition, which will cause the VCO to generate unwanted spurs at the fractions ($f_{VCO} \pm NF/Q$) of the comparison frequency (f_{COMP}). The SA8025 has internal circuitry which generates appropriate amounts of current to compensate for the phase error for different NF.

Due to the difference in processing technology, fractional compensation current on the SA8025 will not follow the UMA1005. Experimental results show that the resistor RF has to be between 200 and 600 kΩ for optimum fractional spur suppression. It is recommended to adjust the CN value for the high, the middle and the low channel to minimize the fractional spurs. Then linear interpolation technique can be applied to calculate all the CN values for the rest of the channels. A long “A” word (A1) needs to be sent to change the channel and set the CN value at the same time.

PCB Layout

Since careful PCB layout has a great impact on the performance of the synthesizer, users should pay special attention to the rules in building RF circuits. Here are some tips for the synthesizer board layout:

- Follow the layout in this document or on the demoboard.
- It is important that VCO ground is large in size and coupled immediately to the grounded side of the PCB. Make sure that there is a clean path for the VCO ground to get to the system ground (power supply ground).
- To avoid interference, the lead between the VCO output and the RF input should be kept as short as possible. A 50Ω termination resistor should be placed close to the RF input.
- Digital ground (V_{SS}) and analog ground (V_{SSA}) must be separated on the component side of the board. They have to be large in size on the PCB and coupled immediately to the grounded side of the PCB. Designers should refer to the latter part of this application note for the recommended PCB layout.
- Power supply bypass capacitors (100nF) for all devices should be located close to the devices with short leads.
- V_{SSA} should be separated from the ground of other devices such as VCO and mixer chip (SA602).

LOOP FILTER DESIGN

This section presents the procedure for designing the loop filter. Due to the sampling nature of the phase detector and the delay introduced in frequency dividers, complicated mathematical analysis is required for deriving the loop design formulas. However, to give designers a convenient tool for quick design, a simple design procedure based on linear control theory is given below. The detailed derivation is included in the Appendix.

Figure 7a shows a simple 1 pole + 1 zero passive low-pass filter which is commonly used with the PLL synthesizer whose phase detector output is current. This filter has a pole at 0Hz and a zero at $(1/2\pi\ R_1\ C_1)$Hz. Together with the pole introduced by the VCO, this filter will give a 2nd order type 2 (2 poles at 0Hz) PLL loop, which our design procedure is based upon. The inclusion of C_2, R_2 and C_3 (see Figure 7b) effectively introduces two more poles located far away from the zero. This will provide more attenuation, if necessary, on the spurious sidebands without affecting the 2nd order nature of the loop.

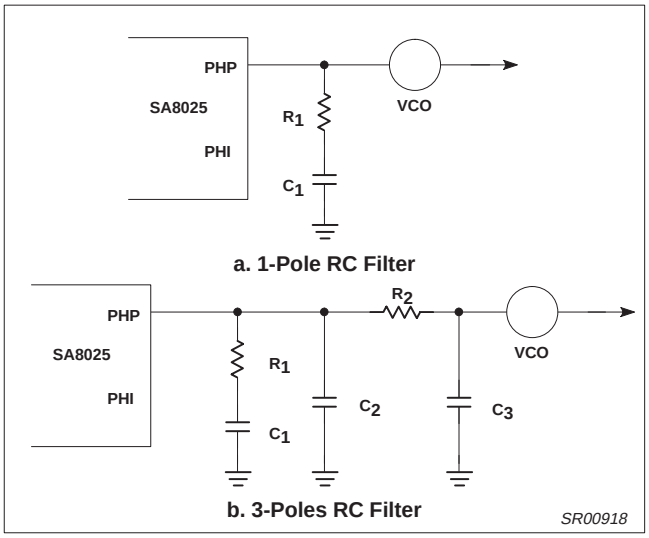

Figure 7. RC Filter Configurations

Definition of the PLL parameters:

δ: final frequency resolution after settling

$$\delta = \frac{\text{frequency error after settling}}{\text{switching step}} \quad \text{(EQ. 16)}$$

t_{SW}: switching time (sec)

f_N: natural frequency of the 2nd order system (Hz), $\omega_N = 2\pi f_N$ (rad/s)

N: total divide ratio

ξ: damping factor of the second order system. Typ. value is 0.707

K_{VCO}: VCO gain (Hz/V) or $2\pi \times$ VCO gain (rad/V)

K_ϕ: phase detector gain = $I_{CP}/2\pi$ (A/rad)

Normal Mode Design

The set of formulas (see Appendix) presented here is valid for normal mode operation in which only charge pump PHP is connected to the low-pass filter. This assumes the STROBE length

is short enough so that speed-up due to STROBE high is minimum in the switching process. Designers should use the normal mode design approach as a starting point and go on to the adaptive mode design if desired PLL performance cannot be met using this configuration.

$$\omega_N = \frac{-\ln(\delta \cdot \xi)}{\xi \cdot t_{SW}} \quad \text{(EQ. 17)}$$

$$C_1 = \frac{K_\phi \cdot K_{VCO}}{N\ \omega_N^{\ 2}} \quad \text{(EQ. 18)}$$

$$R_1 = 2 \cdot \xi \left(\frac{N}{K_\phi \cdot K_{VCO} \cdot C_1}\right)^{0.5} \quad \text{(EQ. 19)}$$

$$C_2 \le \frac{C_1}{10} \quad \text{(EQ. 20)}$$

$$\omega = \frac{1}{C_3 \cdot R_2} \quad \omega \text{ should be at least 10 times larger than } \omega_n \quad \text{(EQ. 21)}$$

NOTE: The unit of the factor $K_\phi \times K_{VCO}$ is unity when all the variables are expressed in radians. Therefore, designers can simply multiply the charge pump output current (I_{CP}) with the VCO gain in Hz/V to obtain this factor.

Adaptive Mode Design

The adaptive mode allows designers to take advantage of having one filter with two different loop filter responses. When the synthesizer is switching from channel to channel, a wider filter bandwidth (speed-up) is desired. Once the loop is locked at the correct frequency, a narrower filter is required to achieve lower noise. This mode can be realized by connecting the PHI charge pump to the integrating capacitor C1 (see Figure 8), controlling the width of the STROBE (amount of time for speed-up), and programming the CK and CL registers. Due to this configuration, the zero of the filter gets multiplied by $[2^{CL+1}\ (CK + 1) + 1] / [1 + 2^{CL+1}]$ times, which makes the loop more stable in speed-up mode. One drawback of this design is that switching from speed-up to normal current will cause a difference in the final phase error due to different current gain, which results in frequency instability or a "glitch" in the frequency domain. Because of this effect, the actual switching time will be longer than what the speed-up loop is designed for, since the loop has to re-settle again due to the glitch. Experimental trial of the width of the STROBE can help alleviate this problem.

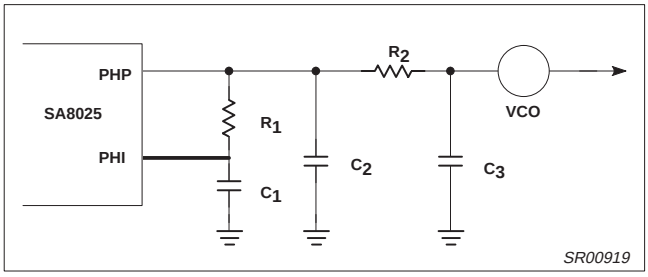

Figure 8. Adaptive Filter

Definition:

ξ_S: speed-up mode damping ratio

ξ_N: normal mode damping ratio

ω_{NS}: speed-up mode natural frequency

ω_{NN}: normal mode natural frequency

Design Steps:

1. Calculate ω_{NS} to meet the system switching time requirement using Eq. 17.
2. Decide how many times ω_{NN} is smaller than ω_{NS}. 5 times will be a good number.
3. Calculate filter component values using Eq. 17 to Eq. 20.
4. Calculate CL and CK values according to

$$CL = 3.32 \log_{10}\left(\frac{\xi_s \cdot \omega_{NS}}{\xi_N \cdot \omega_{NN}} - 1\right) - 1 \quad \text{(EQ. 22)}$$

$$CK = \left[\frac{\left(\frac{\omega_{NS}}{\omega_{NN}}\right)^2 - 1}{\left(\frac{\xi_S \cdot \omega_{NS}}{\xi_N \cdot \omega_{NN}} - 1\right)}\right] - 1 \quad \text{(EQ. 23)}$$

The above procedure ensures the loop bandwidth in speed-up mode is 5 times greater than that in normal mode while maintaining the required stability of the loop.

DESIGN EXAMPLE

This section shows a design example using the SA8025 for the Personal Handy Phone System (PHS), where the device is used in the normal mode (only PHP charge pump is active). The system parameters are as follows:

VCO frequency (f_{VCO}) = 1646.7 to 1670.1MHz

Channel spacing (f_{CH}) = 300kHz

Comparison frequency (f_{COMP}) = 8 × 300kHz = 2.4MHz

Switching time (t_{SW}) = 500µs

Switching step = 25MHz

Frequency error = within 1kHz

VCO gain (K_{VCO}) = 15MHz/V

Reference Crystal (f_{REF}) = 19.2MHz

Determine total divide ratio N

To synthesize channels from 1646 to 1670MHz with f_{COMP} = 2.4MHz, N should be between 686 and 695. For the same loop components, larger N yields smaller natural frequency (f_N). So, jumping from high-end to low-end (larger N) is slower than from low-end to high-end (smaller N). To ensure the same switching time from either direction, we use N = 695 for the worst case.

Determine ω_N

Using Eq. 16

$$\delta = \frac{1000}{25e6} = 0.04e\text{-}3$$

Pick ξ = 0.707 and use t_{SW} = 400µs for safety.

Using Eq. 17

$$\omega_N = \frac{-\ln(0.04e\text{-}3 \cdot 0.707)}{0.707 \cdot 400e{-}6} = 37,035$$

Determine R_N and I_{CP}

Pick RN = 10kΩ and CN = 100. Referring to Figure 5, I_{RN} becomes 80µA when V_{DDA} = 3V.

Using Eq. 1

$$I_{CP} = 100\left(\frac{80e\text{-}6}{32}\right) = 250\mu A$$

Determine R_1, C_1 and C_2
Using Eq. 18 with 2π's from K_{VCO} (rad/V) and K_ϕ (A/rad) cancel out

$$C_1 = 15e6 \left(\frac{250e\text{-}6}{695 \cdot 37,035^2} \right) = 3.93nF$$

Using Eq. 19

$$R_1 = 2 \cdot 0.707 \cdot \left(\frac{695}{15e6 \cdot 250e\text{-}6 \cdot 3.9e\text{-}9} \right)^{0.5} = 9.7k\Omega$$

Using Eq. 20

$$C_2 = \frac{3.93e\text{-}9}{10} = 390pF$$

Determine R_2 and C_3
R_2 and C_3 can help attenuate the unwanted fractional spurs at 300kHz offset.
Using Eq. 21

$$\omega = \frac{1}{R_2 \cdot C_3} \geq 10\omega_N$$

Pick R_2 = 18kΩ, then C_3 = 150pF.

Fractional spurs compensation, if necessary
With f_{COMP} = 300kHz, there would be some spurs located at 300kHz or multiples of 300kHz when NF not equal to 0. For this particular design, we are able to use a fixed CN value (100) to achieve spurs suppression of at least -64dBc for spurs located at 300kHz carrier offset. Spurs located at other frequencies are not present.

Design results

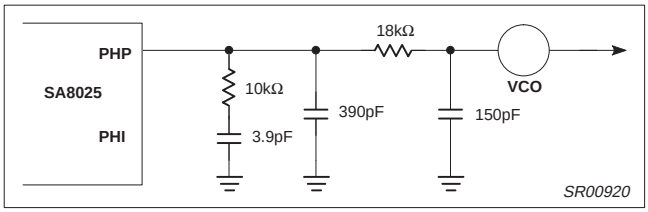

Figure 9. Main Loop Filter

Component values used on the demoboard:
C31 = 3.9pF
R23 = 10kΩ
C32 = 390pF
R24 = 18kΩ
C33 = 150pF
R21 = 560kΩ (RF)
R22 = 10kΩ (RN)

Software setting:
CN = 100
STROBE = 190µs

MEASUREMENT RESULTS

The major performance parameters for a PLL synthesizer are close-in phase noise, spurious sidebands and switching time. This section presents the measurement results obtained from the design made in the section on LOOP FILTER DESIGN.

Close-In Phase Noise

The close-in phase noise level directly correlates with the residual FM and integrated jitter performance, two integrated noise parameters. It is measured within the loop bandwidth (the peak of the "hump" around the carrier) at a specified carrier frequency offset, e.g., 1kHz, and it is expressed in -dBc/Hz. Figure 10 displays the result of such a measurement. The carrier is located at 1668.3MHz (NF = 1) and the span is 10kHz. The resolution bandwidth (measurement bandwidth) is 100Hz. Therefore, the close-in phase noise at 1kHz offset is:

= -58.2dBc – 10 log (100)

= -78.2dBc/Hz

Spurious Performance

Figures 11 and 14 show the spurious performance of the highest and the lowest bands of interest with NF = 1 and 7, which are the worst case for fractional spurs. Other spurs within the band are totally compensated.

Switching Time

The switching time (see Figures 15 and 16) was measured using the HP 53310A Modulation Domain Analyzer (MDA) with option 031. Under the TRIGGER Menu of the MDA, "Triggered", "Ext Edge" and "Arm Only" were selected. The instrument was setup to accept an external trigger, which was the STROBE signal used for programming the synthesizer. This signal was connected to the Ext Arm input while the VCO signal was fed into the Channel C. The MDA would display the frequency versus time variation of the VCO signal upon the arrival of the STROBE signal. This design achieved a switching time of 400µs to within 1kHz of the final frequency for a 21.6MHz jump between 1646.7 and 1668.3MHz in either direction. The STROBE width used in this experiment was 190µs.

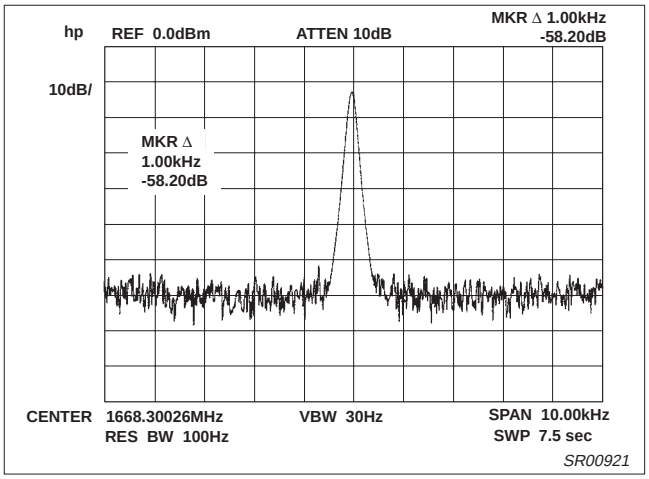

Figure 10. Close-In Phase Noise at 1668.3MHz

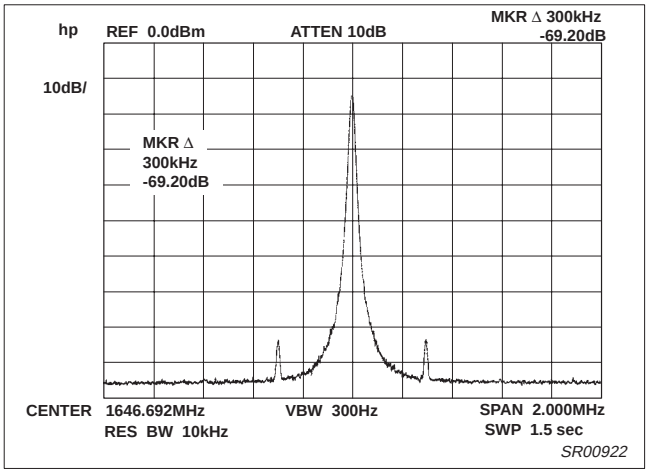

Figure 11. Fractional Spurs (f_{VCO} = 1646.7MHz, NF = 1)

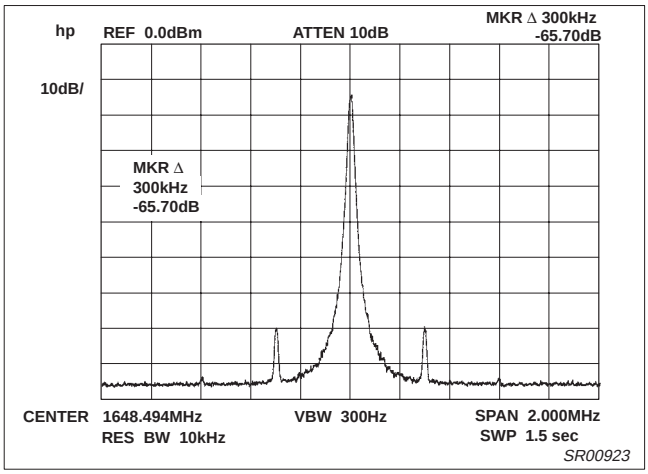

Figure 12. Fractional Spurs (f_{VCO} = 1648.5MHz, NF = 7)

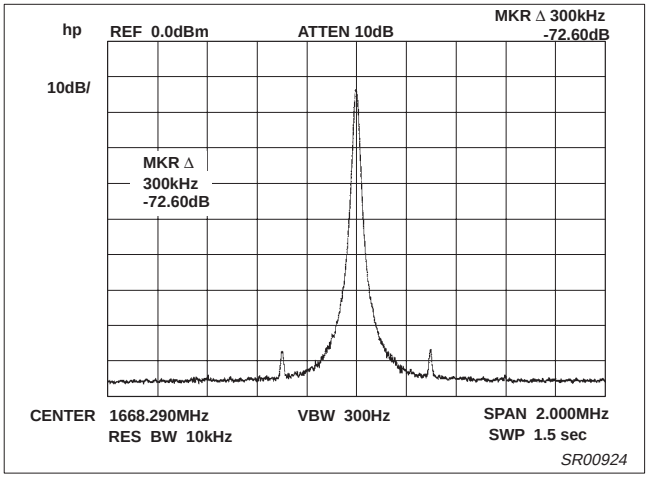

Figure 13. Fractional Spurs (f_{VCO} = 1668.3MHz, NF = 1)

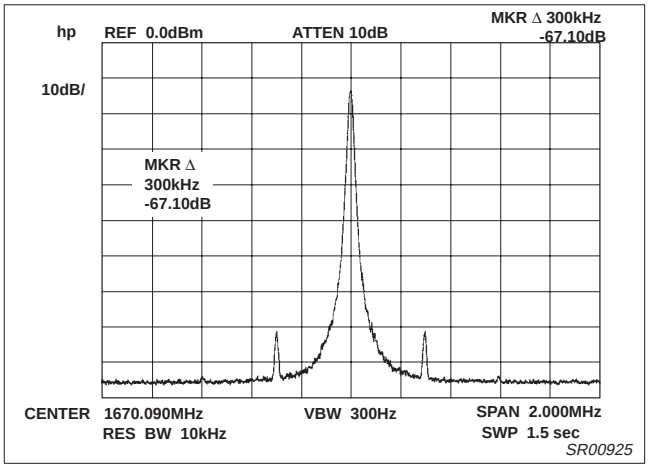

Figure 14. Fractional Spurs (f_{VCO} = 1670.1MHz, NF = 7)

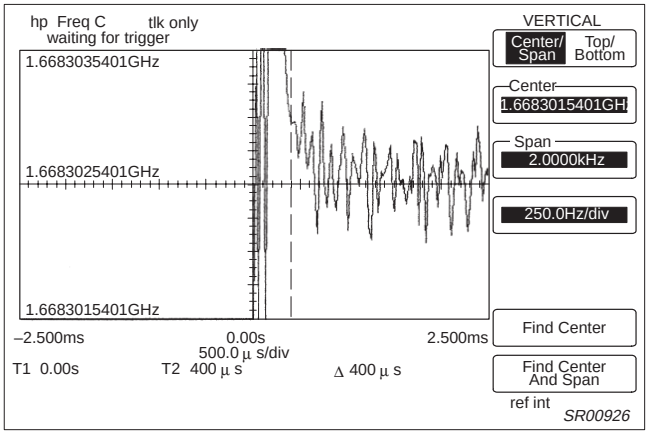

Figure 15. Switching Time (1668.3 to 1646.7MHz Step to Within 1kHz)

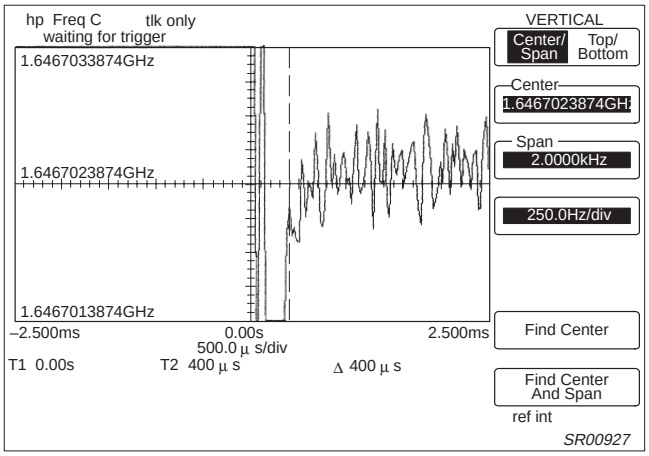

Figure 16. Switching Time (1646.7 to 1668.3MHz Step to Within 1kHz)

MODULO 4 DESIGN

Previous sections showed a design using a 4 modulus prescaler (64/65/68/73) to synthesize total divide ratios (N) from 686 to 694. This requires sending both B and A words since NM4 is stored in B word. In some designs, users may prefer to send only one word for channel switching due to hardware limitation. We could have used modulo 5 (FMOD = 5) to make N five times higher and used a triple modulus prescaler (64/65/68 or 64/65/73). In some situations this is impossible since the comparison frequency has to be an integer factor of the crystal reference. For instance, if f_{REF} is 19.2MHz and f_{CH} is 300kHz, f_{COMP} becomes 1.5MHz, which is not an integer factor of 19.2MHz. To get around this problem, a modulo 4 design must be used.

Figure 17 shows the concept of a modulo 4 design. In the mod 4 case, f_{COMP} is four times the channel spacing, f_{CH}. Instead of programming NF to one through seven, even numbers are used.

To synthesize 1656.3, 1656.6, 1656.9, 1657.2MHz with channel spacing = 300kHz using mod 8 and mod 4.

SA8025 (mod 8)	SA8025 (mod 4)
$f_{VCO} = f_{COMP}$ (N+NF/8)	$f_{VCO} = f_{COMP}$ (N+NF/8)
1656.3 = 2.4 (690 + 1/8)	1656.3 = 1.2 (1380 + 2/8)
1656.6 = 2.4 (690 + 2/8)	1656.6 = 1.2 (1380 + 4/8)
1656.9 = 2.4 (690 + 3/8)	1656.9 = 1.2 (1380 + 6/8)
1657.2 = 2.4 (690 + 4/8)	1657.2 = 1.2 (1381 + 0/8)
f_{COMP} = 8 x f_{CH} = 2.4MHz	f_{COMP} = 4 x f_{CH} = 1.2MHz

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Figure 17.

To achieve the same loop response with the mod 8 design, the same loop filter with twice the charge pump current can be used. This can be derived from Eq. 18. When N is doubled, K_ϕ (two times more current) has to be doubled as well to maintain the same natural frequency which determines the switching time and residual FM. In this case, we use CN = 200 for the mod 4 design.

The only penalty of this method is that theoretical close-in phase noise performance is affected. Since N is twice as much, the close-in noise floor should be 20log(2) = 6dB higher. However, minor degradation for using mod 4 was measured in the laboratory. This could be due to the fact that the comparison cycles are fewer with mod 4, which makes the charge pump ON time less, thus producing less noise. In addition, higher charge pump current improves the phase noise.

MOD 4 DESIGN MEASUREMENT RESULTS

Figures 18 to 22 show the measurement results for the mod 4 design. The close-in phase noise level is shown to be -77.1dBc/Hz at 1kHz carrier offset with a measurement bandwidth of 100Hz. Spurious sidebands (see Figures 19 and 20), which are caused by fractional jitter, are -67dB down from carrier for the high band and -68dB down for the low band. Switching time (see Figures 21 and 22) is exactly the same as the mod 8 design (400µs) because the loop natural frequency is the same for both cases.

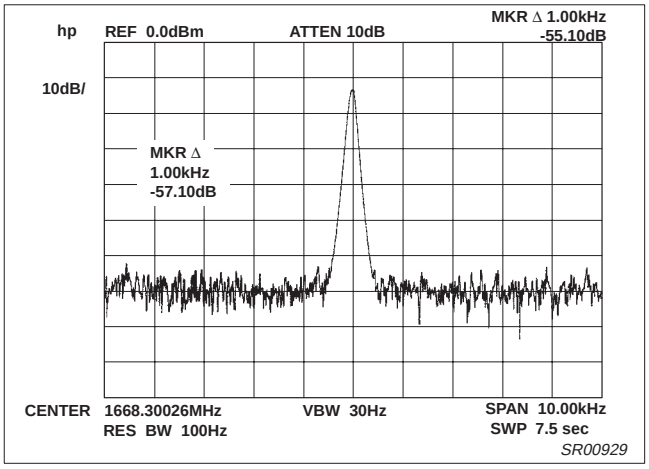


Figure 18. Close-In Phase Noise at 1668.3MHz

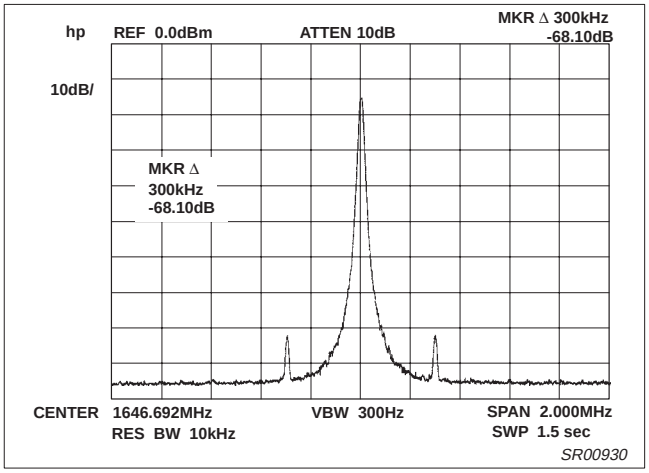


Figure 19. Fractional Spurs (f_{VCO} = 1646.7MHz, NF = 2)

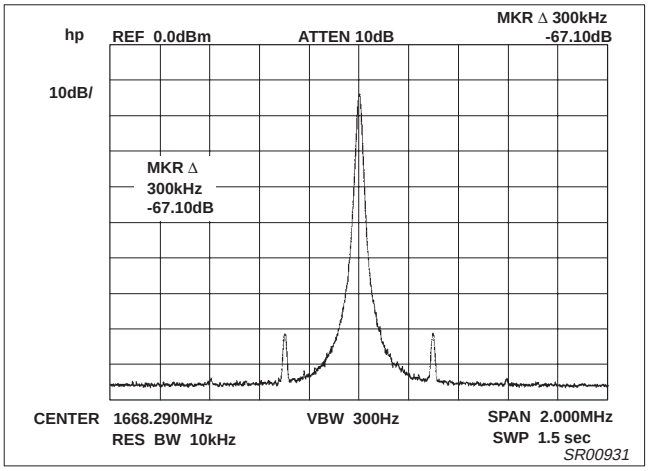


Figure 20. Fractional Spurs (f_{VCO} = 1668.3MHz, NF = 2)

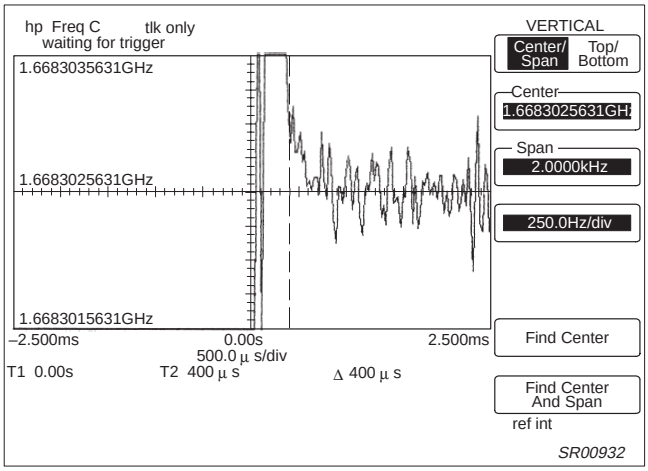


Figure 21. Switching Time (1668.3 to 1646.7MHz Step to Within 1kHz)

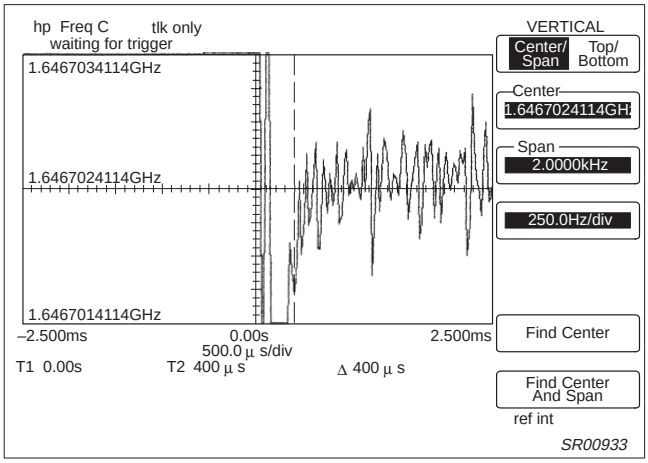


Figure 22. Switching Time (1646.7 to 1668.3MHz Step to Within 1kHz)

FREQUENTLY ASKED QUESTIONS

Q. The part is powered-up and programmed. The VCO is still free-running. What's wrong?

A. Three things to check for if the PLL does not lock:

1. Make sure the correct data have been transmitted to the CLK, DATA and STROBE pins
2. Make sure a reference signal with correct frequency and amplitude are present at the REF_{IN} pin.
3. Make sure that the prescaler value is chosen correctly. The SA8025 has two 3 modulus prescalers and uses different programming bits.
4. Be aware of cold solder joints. Pay special attention to the loop filter section and the connection from the VCO to the RF_{IN} pin.

Q. The synthesizer locks up, but it locks at a wrong frequency. Why?

A. Check the NM1, NM2, NM3 and NM4 bits. Make sure they are correctly programmed.

Q. I see spurs sitting at the comparison frequency offset and they don't change with the filter bandwidth. How can I get rid of them?

A. These spurs may be caused by improper grounding of the VCO and the filter section. Make sure they all have short and clean paths going back to the supply ground. Also, clean the filter section to avoid leakage.

Q. I see some spurs which are neither fractional nor comparison spurs. What are they?

A. Since the VCO is a very sensitive device, it can be influenced by many noise sources. Common ones are:

1. Computer monitor. The sweeping frequency of the screen will modulate the VCO and create spurious sidebands at 30 to 40kHz carrier offset.
2. Free-running auxiliary VCO. Even though the EA bit is disabled, if the auxiliary VCO is still ON, it will modulate the main VCO and cause spurs.
3. Fluorescent lamp.

Q. How can the residual FM be improved?

A. Three things can be done to improve residual FM:

1. Use a narrower loop filter.
2. Use a higher crystal reference frequency. This will reduce the charge pumps ON time and make the charge pumps generate less noise.
3. Use higher charge pump output current. This will increase the signal to noise ratio at the charge pump, which makes the circuit less noisy.

Q. When I FM modulate the AUX synthesizer, I see modulation on the MAIN carrier as well. Is that normal?

A. Yes, that is normal. The amount of interference between the AUX and the MAIN has to be verified experimentally.

Q. If I double the phase detector gain (twice the current), what should be done to keep the switching time the same?

A. Referring to Eq. 18 and Eq. 19, the value of C_1 should be doubled and R_1 should be halved if you want to maintain the same natural frequency of the loop when the detector gain (K_ϕ) is twice what it was before.

Q. When I use the 3 modulus prescaler (PR = 10), what should the values for NM4 be?
A. Simply treat them as "don't cares".

Q. What is the phase detector gain? Is it charge pump output current divided by 2π or just the charge pump output current, itself?
A. The phase detector gain (K_ϕ) is equal to the charge pump output current (I_{CP}) divided by 2π since the phase detector covers 2π range. However, when we use the design formulas shown in the "Loop Filter Design" section, K_ϕ can be replaced directly by I_{CP} because the 2π factor will be cancelled out by the 2π from the VCO gain, K_{VCO}.

Q. What should I do with the RA and PHA pins when the auxiliary synthesizer is not used?
A. When the auxiliary synthesizer is not used, leave PHA open, connect AUX_{IN} to ground, connect RA to V_{DDA} or leave it open and program EA bit to zero.

Q. Variations on the RF pins input impedance for different prescaler value can cause VCO pulling. Does that happen to the SA8025?
A. The RF input to the prescaler is well buffered, and the input impedance should always stay the same.

Q. Can the clock signal be disconnected after the A word is sent?
A. Yes, the clock signal can be disabled after the A word is sent and enabled again for sending new words to the part.

Q. Can I drive the part with a +5dBm RF signal even though the spec is 0dBm max?
A. Users should refer to the graphs put in the latter part of the data sheet for minimum and maximum input power. The device should be able to handle +5dBm at 1800MHz, but this is not guaranteed in the data sheet.

Q. I am doing open-loop modulation on the main synthesizer. How do I put the charge pump to high impedance state to allow modulation?
A. Program CN register to zero. This will set the charge pump to a high output impedance state so that FM modulation can be done.

Q. Is the demoboard layout good for any applications? If not, what should I do?
A. The demoboard layout included in this document was optimized only for this particular design. Designers should consult the PCB layout hints in the "PCB Layout" section of this application note when laying out circuit boards for other applications.

Q. I am using the S8025 for PHS system and seeing different amplitudes on the fractional spurs from part to part. However, this variation does not appear to affect my RX/TX performance. Is this a safe assumption?
A. Yes, because the SA8025 is targeted for the PHS system and any spurs that only fall in the adjacent channels (at 300kHz carrier offset) are acceptable for the PHS.

REFERENCES

"Digital PLL Frequency Synthesizers", Ulrich L. Rohde, Prentice Hall, 1983.

"Designer Guide to Frequency Synthesis Using the UMA1005", Application Note, Report No: SCO/AN92002.

"Modem Control Systems", Richard C. Dorf, Addison Wesley, 1989.

APPENDIX

Derivation of the 2nd order PLL design formula:

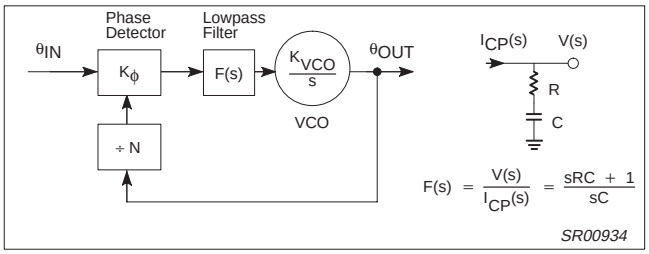


Figure 23. PLL Block Diagram

The transfer function of the loop low-pass filter is represented by:

$$F(s) = \frac{sRC + 1}{sC} \quad \text{(EQ. 24)}$$

The low-pass filter has a pole at 0Hz (set denominator to zero) and a zero at 1/2πRC Hz (set numerator to 0).

Referring to Figure 23, the open-loop response of the system (multiplication of the Forward Gain and Feedback Gain) becomes:

$$G(s)H(s) = \frac{K_\phi \cdot K_{VCO}}{Ns}\left(\frac{sRC + 1}{sC}\right) \quad \text{(EQ. 25)}$$

Phase Margin (ϕ_{PM}) is defined as the difference between -180° and the phase at the point where the open-loop response has unity gain. A stable system must have a ϕ_{PM} greater than 0°. Eq. 25 shows that there are two poles sitting at 0Hz, one from the filter and one from the VCO, which causes -180° phase shift. In order to have a stable system, a zero has to be added to the filter so that ϕ_{PM} will be greater than zero. ϕ_{PM} is related to the damping factor, ξ, with $\xi = 0.01 \times \phi_{PM}$.

To find the characteristic equation (CE) of the system, we equate 1 + G(s)H(s) to zero. Therefore,

$$1 + \frac{K_\phi \cdot K_{VCO}\,(sRC + 1)}{s^2NC} = 0 \quad \text{(EQ. 26)}$$

The CE becomes

$$s^2 + \frac{K_\phi \cdot K_{VCO} \cdot R}{N}\,s + \frac{K_\phi \cdot K_{VCO}}{NC} \quad \text{(EQ. 27)}$$

Compare Eq. 27 with the standard 2nd order CE ($s^2 + 2\zeta\omega_N s + \omega_N^2$), we have

$$\omega_N^2 = \frac{K_\phi \cdot K_{VCO}}{NC} \quad \Rightarrow \quad C = \frac{K_\phi \cdot K_{VCO}}{N\,\omega_N^2} \quad \text{(EQ. 28)}$$

$$2\xi\omega_N^2 = \frac{K_\phi \cdot K_{VCO} \cdot R}{N} \Rightarrow R = 2 \cdot \xi \left(\frac{N}{K_\phi \cdot K_{VCO} \cdot C}\right)^{0.5} \quad \text{(EQ. 29}$$

which are the design used in "Loop Filter Design" section.

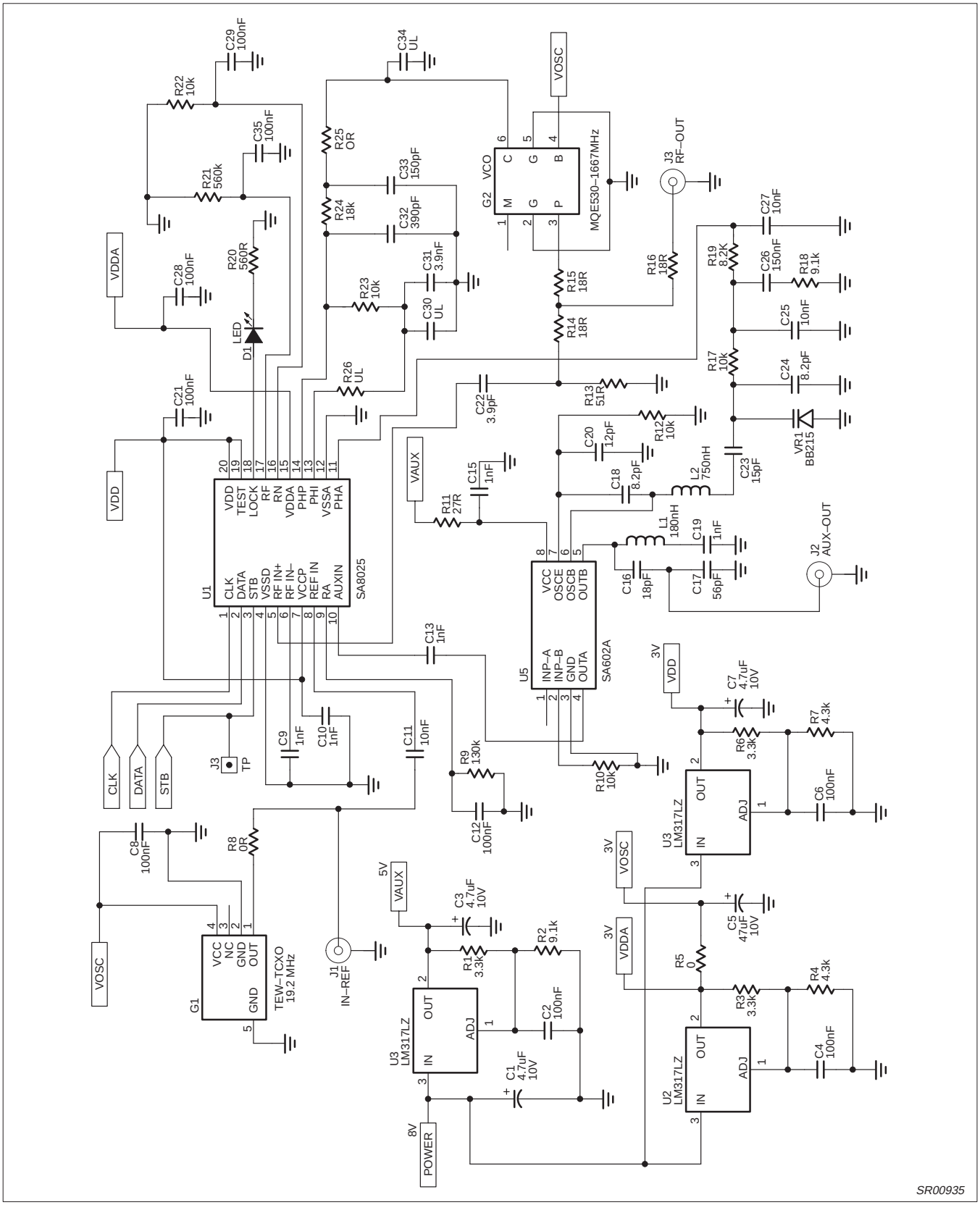
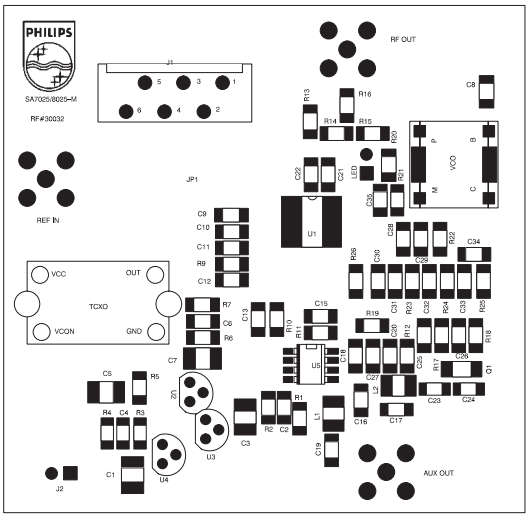
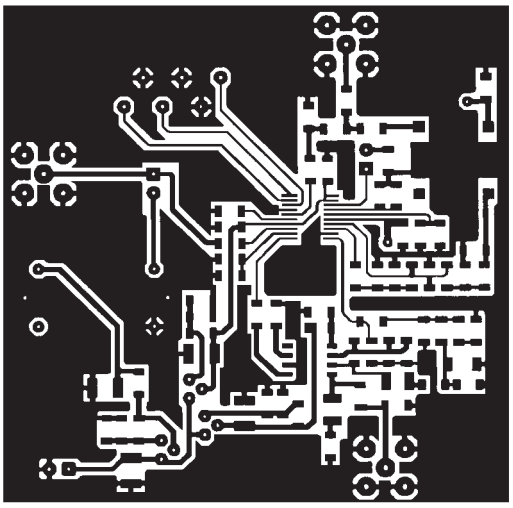


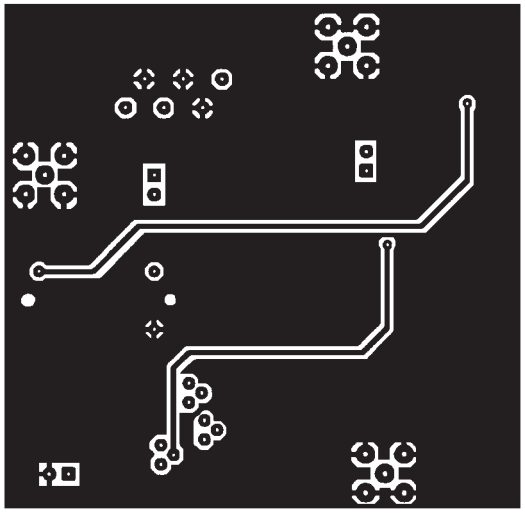
Figure 24. SA8025DK Application Circuit



TOP SILK SCREEN



TOP VIEW



BOTTOM VIEW

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Figure 25. SA8025DK Demoboard Layout (NOT ACTUAL SIZE)

Table 2. Customer Application Component List for SA8025DK

Qty.	Part Value	Volt	Part Reference	Part Description	Vendor	Mfg	Part Number
Surface Mount Capacitors							
1	3.9pF	50V	C22	Cap. cer. 1206 NPO ±0.5pF	Garrett	Rohm	MCH315A3R9CK
2	8.2pF	50V	C24, C18	Cap. cer. 1206 NPO ±0.5pF	Garrett	Rohm	MCH315A8R2CK
1	12pF	50V	C20	Cap. cer. 1206 NPO ±5%	Garrett	Rohm	MCH315A120JK
1	15pF	50V	C23	Cap. cer. 1206 NPO ±5%	Garrett	Rohm	MCH315A150JK
1	18pF	50V	C16	Cap. cer. 1206 NPO ±5%	Garrett	Rohm	MCH315A180JK
1	56pF	50V	C17	Cap. cer. 1206 NPO ±5%	Garrett	Rohm	MCH315A560JK
1	150pF	50V	C33	Cap. cer. 1206 NPO ±5%	Garrett	Rohm	MCH315A151JK
1	390pF	50V	C32	Cap. cer. 1206 NPO ±5%	Garrett	Rohm	MCH315A391JK
5	1000pF	50V	C9, C10, C13, C15, C19	Cap. cer. X7R ±10%	Garrett	Rohm	MCH315A102JP
1	3900pF	50V	C31	Cap. cer. X7R ±10%	Garrett	Rohm	MCH315C392KK
3	0.01µF	50V	C11, C25, C27	Cap. cer. X7R ±10%	Garrett	Rohm	MCH315C103KK
9	0.1µF	50V	C2, C4, C6, C8, C12, C21, C28, C29, C35	Cap. cer. X7R ±10%	Garrett	Rohm	MCH315C104KP
1	0.15µF	16V	C26	Cap. cer. X7R ±10%	Garrett	Rohm	MCH315C154KP
4	4.7µF	10V	C1, C3, C5, C7	Tant. chip cap. A 3216 ±10%	Garrett	Philips	49MC475B010KOAS
Surface Mount Resistors							
3	0Ω		R5, R8, R25	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW000E
3	18Ω		R14, R15, R16	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW180E
1	27Ω		R11	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW270E
1	51Ω		R13	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW510E
1	560Ω		R20	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW561E
3	3.3kΩ		R1, R3, R6	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW332E
2	4.3kΩ		R5, R8, R25	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW432E
1	8.2kΩ		R19	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW822E
2	9.1kΩ		R2, R18	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW912E
5	10kΩ		R10, R12, R17, R22, R23	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW103E
1	18kΩ		R24	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW183E
1	130kΩ		R9	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW134E
1	560kΩ		R21	Res. chip 1206 1/8W ±5%	Garrett	Rohm	MCR18JW564E
Surface Mount Diodes							
1			VR1 (Varactor)	Variable capacitance SMD diode	Digikey	Philips	BB215
1			D1	SM Led	Digikey		
Surface Mount Inductors							
1	0.18µH		L1	Inductor SM Mold/WW A	Garrett	J.W. Miller	PM20-R18M
1	0.75µH		L2	Inductor SM Mold/WW A	Garrett	J.W. Miller	PM20-R68M
Voltage Regulators							
3			U1, U2, U3	Voltage regulator	Digikey		LM317LZ
TCXO							
1	19.2MHz		G1	Temp. controlled crystal osc.	TEW	TEW	TXS1034N-19.2MHz
VCO							
1	1667MHz		G2	Voltage controlled osc.	Murata	Murata Erie	MQE530-1667
Surface Mount Integrated Circuits							
1			U4	1MHz Fractional-N Synthesizer	Philips	Philips	SA8025DK
1			U5	Double Balanced Mixer Oscillator	Philips	Philips	SA602A
Miscellaneous							
3			SMA1, SMA2, SMA3	SMA right angle jack receptacle	Newark	EF Johnson	142-0701-301
1			J1	Male 6-pins connector	STOCKO	STOCKO	MKS1956-6-0-606
1			J2	Male 2-pins connector	STOCKO	STOCKO	MKS1851-6-0-202
1			JP1	Test point	Digikey	3M	929647-36
1				Printed circuit board	Philips	Philips	SA7025/8025-M
75 Total Parts							